Applicant: Carl Cooper
Serial No: 08/486,000
File Date: June 8, 1995
Invention: IMPROVED PROGRAM VIEWING APPARATUS AND METHOD

Examiner: Rao, S.
Art Unit: 2613

1717 East Ninth Street
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April 8, 1997

COMMISSIONER OF PATENTS
AND TRADEMARKS
Washington, D.C. 20231

D E C L A R A T I O N

Dear Commissioner:

My name is Steve Anderson.

I reside at 21886 Hyannisport Drive, Cupertino, California 95014.

I am employed at Signal Dynamics Corporation located at 2336 B Walsh Avenue, Santa Clara, California 95051.

I am the co-inventor of U.S. Application Serial 08/322,069 filed October 12, 1994 together with its continuation U.S. Application Serial 08/486,000 filed June 8, 1995 entitled Improved Program Viewing Apparatus And Method.

Unless stated otherwise, all of the below described activities describe my work on the audio delay and pitch shifting part of the invention, as discussed in the prior application for a frequency convertor system.

As a co-inventor, I began working on the invention on or before January 14, 1993.

On January 28, 1993, I summarized my work on the project leading to an embodiment of the invention beginning on January 14, 1993 and extending through January 24, 1993.

During this time period, I began my initial work into the block diagram and flow charting for the device (EX A).

Between the dates of January 25, 1993 and February 7, 1993, I further worked on the invention and the various complexities of design (EX B).

Between February 8, 1993 and March 7, 1993, this work included developmental work in the SPROC description language as put forth by Star Semiconductor. This SPROC implementation was to be included in the design effort (EX C).

From March through April, 1993, I worked on the SPROC language in a related delay detector project. This included the use of custom cells in order to reduce the amount of instructions for the implementation.

Between March 8, 1993 and May 2, 1993, I continued work on developing an understanding of the scope of the project including the possibility of fitting the processing onto a single SPROC chip (EX D). At this time, a pitch corrector code existed which could be reduced through this cell consolidation.

Between May 17, 1993 and May 23, 1993, I continued to work on the SPROC board in the related delay detector project including interface characteristics and sample per line (EX E).

On June 2, 1993, I completed my initial estimate of the SPROC portion of the project implementing the invention. This included using the then present pitch corrector code albeit consolidated by cascading cells and eliminating unused functions (EX F).

Between the time period of May 3, 1993 and May 30, 1993 I continued my work on the scope of the project (see EX G).

Between May 31, 1993 and June 6, 1993, I continued my work on the scope of the project which included the delay increment changes, the outside world interfaces, and the processor interfaces for the design (EX H).

On June 11, 1993, I had a rough schematic prepared for the audio delay memory and DSP parallel port interface (EX I).

Between June 7, 1993 and June 13, 1993, I further worked on the schematic of the circuit, including obtaining more information about the SPROC cells (EX J).

On June 18, 1993, I noted that changes in the hardware breadboard may become necessary because of code changes (EX K).

Between June 14 and June 20, 1993, I continued to work on the cell coding (EX L).

Between June 21 and June 27, 1993, I continued to work on cell coding with a need to develop some parallel port hardware to continue (EX M).

On June 28 and 29, 1993, I attended the Star Semiconductor Cell Development course at Marshall Industries in Milpitas, California in furtherance of the invention.

Between June 28, 1993 and July 4, 1993, I continued testing the SPROC code for the related delay detector project (EX N).

Between July 5 and July 11, 1993, I continued testing and debugging the breadboard of the related delay detector project (EX O).

Between July 12 and July 18, 1993, I continued testing and debugging the breadboard, including running tests on the internal and external signal sources, of the related delay detector project (EX P).

On July 22, 1993, I faxed a phase shifter signal control diagram to Carl Cooper at his request (EX Q).

Between July 19, 1993 and July 25, 1995, I continued testing and debugging the breadboard of the related delay detector project (EX R).

Between July 25, 1993 and November 28, 1993, I continued working on the schematics in order to develop a production type device in the related delay detector project. During this period I also acquired needed test equipment as well as sending microprocessor interface specifications out for implementation by an outside supplier.

Between November 29, 1993 and December 5, 1993, I worked further in respect to this production type device in the related delay detector project including debugging the unit (EX S).

Between December 6, 1993 and December 12, 1993, I completed a review of the SPROC custom cell code and programmed an EPROM to verify the design would work from PROM in the related delay detector project. The unit was in addition subject to possible future code modification (EX T).

Between December 23, 1993 and January 2, 1994, I completed the schematic for the breadboard memory and additional parts of the circuitry for the device (EX U).

Between January 3, 1994 and January 9, 1994, I completed the schematic markup and submitted some schematics for outside construction. I further worked with the interface and registers (EX V).

Between January 10, 1994 and January 16, 1994, I assisted with the alternate part selection for some of the breadboard parts and began modifying the SPROC code to conform with the current design (EX W).

Between January 24, 1994 and February 6, 1994, I continued my work in respect to modifying the SPROC code (EX X).

Between February 14, 1994 and February 20, 1994, I began testing the memory breadboard and some modifications of another related board. I in addition waited for the completion of certain work from outside suppliers (EX Y).

Between February 28, 1994 and March 6, 1994, I continued with the development of the implementation of the project including hardware test and debug and code debug (EX Z).

Between March 7, 1994 and March 13, 1994, I continued the testing and debugging of the breadboard implementation of the project this included getting the triple mode stretch cells working well enough to begin to put all cells together (EX a).

Between March 14, 1994 and April 10, 1994, I continued the SPROC code testing and debugging. I further

obtained a two way pitch shifting implementation for the device (EX b).

Between April 11, 1994 and April 17, 1994, I continued my testing and debugging (EX c).

Between April 18, 1994 and April 24, 1994, I had a substantially successful integration of delay, pitch correction, and control. I further worked to add a third track to the stretch cells (EX d).

Between April 25, 1994 and May 1, 1994, I obtained a fully functional implementation of the device. I modified the extrapolation and the stretch and delay cells to improve the quality of the device (EX e).

Between May 2, 1994 and May 29, 1994, I continued the code development and improved sample delay mismatches. I further began researching design modifications, especially in respect to the serial digital audio interface (EX f).

Between May 30, 1994 and June 5, 1994, I prepared a six second memory breadboard schematic and updated description of block diagrams of the latest SPROC implementation (EX g).

Between June 6 and June 12, 1994, I continued reading the data sheets in respect to various chips in order to develop an understanding of the serial digital audio and sample rate conversion interfaces. Solved delay problem on the main breadboard (EX h).

Between June 20 and June 26, 1994, I continued with the design for the interfaces, including the possibility of the microprocessor interface and the analog to digital conversion (EX i).

Between June 27, 1994 and July 3, 1994, I developed a list of various components in order to approximate the parts cost required to improve the implementation to 20 bits from 16. In addition, I began modification and test of the code in the SPROC system for a six second delay (EX j).

Between July 4 and July 10, 1994, I continued modification of the code and the interpolation factors including the delay cell (EX k).

On July 25, 1994, I reported to Carl Cooper of the component cost differences for the various alternatives of the audio delay (EX l).

Between July 11, 1994 and August 7, 1994, I furthered my work in respect to the digital to analog converter, the 20 bit cost differential, and the SPROC code implementation of a single memory single cell stretch/compress cell (EX m).

Between August 8 and August 14, 1994, I continued my work on the device including the SPROC code development and ramp fade generation (EX n).

Between August 15 and August 21, 1994, I continued the SPROC code development and debugging of the differential delays (EX o).

Between August 22 and August 28, 1994, I worked further on the SPROC code development including optimization of the splice qualification processing (EX p).

On September 1, 1994, I reported to Carl Cooper in respect to the analog/digital converters and the various costs in respect thereto, these costs having previously been developed by myself (EX q).

Between August 29, 1994 and September 4, 1994, I continued my work on the digital to analog converters and the analog to digital converter sections. I also worked on the splice quality dependency on the amplitude match (EX r).

Between September 5 and September 11, 1994, I worked further in respect to the data converter analog interface circuits (EX s).

Between September 12, 1994 and October 23, 1994, I continued the design implementation and component selection for the data converter interface circuits. I further modified the breadboard in order to make more memory available (EX t).

Between October 24 and October 31, 1994, I further worked in respect to the operational amps and the splice match for the device (EX u).

On October 12, 1994, U.S. Application Serial 08/322,069, the frequency converter parent application, was filed.

On November 2, 1994, I reported to Carl Cooper in respect to the potential unavailability of the particular Star Semiconductor SPROC chips that I had incorporated into the design (EX v).

On November 4, 1994, I communicated with Carl Cooper in respect to acquiring design audio serial interface specs in addition to the EBU tech 3250 together with the need to acquire these additional specs (EX w).

Between November 7 and November 13, 1994, I further worked in respect to the implementation of the invention including various test results in respect thereto (EX x).

Between November 14 and November 20, 1994, I ran tests on the algorithm (EX y).

On November 28, 1994, I completed an overview of the project together with the status of the various components including the terminal display, user data HDLC port, and remote control (EX z).

Between November 21 and November 27, 1994, I completed a block diagram of the AES/EBU transmit frequency synthesizer (EX I).

Between November 28, 1994 and December 4, 1994, I continued testing the SPROC code (EX II).

On December 8, 1994, I prepared a preliminary block diagram and integrated circuit complement estimate (EX III).

Between December 5 and December 11, 1994, I completed a preliminary function specification and began preparing a schedule for the commercial implementation of the device (EX IV).

Between December 12 and December 18, 1994, I further worked in respect to the device including the various features available including a microcontroller interface (EX V).

Between December 19 and December 25, 1994, I worked further in respect to the interface (EX VI).

On December 23, 1994, I prepared a report to Carl Cooper in respect to the status of the device (EX VII).

On December 27, 1994, I followed up according to Carl Cooper in respect to the standards applicable to the device and the control and display characteristics (EX VIII).

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on

information and belief are believed to be true, and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both under section 101 of Title 18 of the USC and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

4/16/97
Date

Steve Anderson